What is claimed is:

Sub A1

1. An active matrix liquid crystal display apparatus, comprising:

a plurality of pixels including switching transistors each having a gate electrode, a first electrode and a second electrode connected to a pixel electrode;

a plurality of data signal lines connected to the second electrode associated with any one of the transistors;

a plurality of gate signal lines connected to the gate electrode associated with any one of the transistors; and

a gate driver connected to the plurality of gate signal lines, said gate driver receiving first and second voltages and outputting any one of the first and second voltages in such a manner to drive the gate signal lines sequentially, said first voltage changing prior to exciting of successive gate signal lines.

2. The active matrix liquid crystal display apparatus as claimed in claim 1, wherein the first voltage drops prior to exciting of the successive gate signal lines.

3. The active matrix liquid crystal display apparatus as claimed in claim 1, wherein the first voltage drops exponentially.

4. The active matrix liquid crystal display apparatus as claimed in claim 1, wherein the first voltage drops linearly.

5. The active matrix liquid crystal display apparatus as

claimed in claim 1, wherein the first voltage drops stepwise.

6. The active matrix liquid crystal display apparatus as claimed in claim 1, wherein a minimum value of the first voltage is higher than a maximum value of the second voltage.

7. A method of driving an active matrix liquid crystal display apparatus including pixels positioned at intersecting points of gate lines with signal lines and having thin film transistors connected to the gate lines and the signal lines, and a gate driver connected to the gate line and having a shift register, said method comprising the steps of:

inputting a first voltage and a periodically changing second voltage;

supplying the second voltage, via a switching device, to the gate line; and

supplying the first voltage, via the switching device, to the gate line, said switching device being controlled by the shift register, wherein a minimum value of the second voltage is higher than a maximum value of the first voltage.

8. The method as claimed in claim 7, wherein the first voltage is supplied to the gate line during a time interval when the thin film transistors connected to the gate lines are turned on.

9. The method as claimed in claim 7, wherein the shift register operates at a driving voltage having a logical voltage level.

Add B1

Add C1

Add D1